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SAXENA, AKASH

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,689	RICH ET AL.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been presented for examination based on the application filed on 2nd January 2002.

Specification

2. Disclosure is objected to for the following informalities:
   a. The specification incorporates by reference of two co-pending/issued applications. Specification should be updated to provide the Patent No./Application No. of the references.
   b. The specification (Pg.22, Line 1) discloses, "typical tuple $X_1Y_1Z_1$ for a two input AND gate". According to disclosed convention (Pg.21, line 19) the correct order of the tuple should have been $Z_1X_1Y_1$.
   c. The specification (Pg.22, Line 24) discloses, "4/byte/slot". By disclosed convention the correct term should have been "4 bytes/slot". Appropriate corrections are required.

Claim Objection

3. Claims 1-6 are objected to, as the preamble should state the intended use or objective of the claimed invention. Appropriate action is required.

Claim Interpretation

4. Claim 1: "tpd_super_rise_time" and "tpd_super_fall_time" are interpreted as rise time and fall time because the claim language does not provide any detailed definition of these generic variables.

   Further, claim 1 contains minor informalities: the step of initializing lacks proper punctuation marks. Examiner interprets the step of "initializing" as follows: "initializing other generic variables, corresponding to every VHDL gate model in the VHDL technology library, to an equation representing a correlation policy;"

Claim Rejections - 35 USC § 112 ¶ 1st

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Although the claim does not employ means-plus-function language explicitly, claim 3 recites a single step claim. The step of "binding correlated delay constants in a 3 dimensional variable data array structure..." can have many possible embodiments and only one is disclosed in the specification.

   MPEP 2164.08(a) states:

> A single means claim, i.e., where a means recitation does not appear in combination with another recited element of means, is subject to an undue breadth rejection under 35 U.S.C. 112, first paragraph. In re Hyatt, 708 F.2d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983) (A single means claim, which covered every conceivable means for achieving the stated purpose was held nonenabling for the scope of the claim because the specification disclosed at most only those means known to the inventor.). When claims depend on a recited property, a fact situation comparable to Hyatt is possible, where the claim covers every conceivable structure (means) for achieving the stated property (result) while the specification discloses at most only those known to the inventor.

Claim Rejections - 35 USC § 112 ¶ 2nd

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention.

Regarding Claim 1, 6, 7, 10, 12 & 15

In the specification (summary), applicant has stated that his invention is to bind correlated delay constants in a 3-dimensional variable data array structure to a VHDL technology library using a VHDL package embedded with the correlation delay data with a motivation to speed up simulation and reduce the model size (Pg 4 Lines 5-13). The method of claim 1, as written, does not claim the invention as disclosed in the specification (pages 4-5) and additionally the steps of the methods do not claim the invention.

Regarding Claim 3

The method of claim 3, as written, does not sufficiently disclose the subject matter of the applicant's invention. It is not clear whether the applicant regard the process of binding, or the process of creating correlation between delay constants, or the 3-dimensional variable data array as his invention. Further, there is an insufficient detail in structure of the method claim (missing steps) to clearly identify claimed invention.

Independent claims 6, 7, 10, 12 & 15 suffer from the similar deficiency as claim 1 and rejected for the same reasons.

Claims 2, 4-5, 8-9, 11, 13-14 are rejected based on their dependency on their respective independent claims rejected above.

7. **Claims 3-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

Regarding Claim 3

The method of claim 3, as written, does not disclose what correlated delay constants means, i.e. what are they correlated to. Further, there is no disclosure of how the correlated delay constants are correlated and how the binding is done with the technology library. Claims 4 & 5 are rejected on basis of their dependency on claim 3.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 1-6 & 10-11 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Regarding Claim 1

The method of claim 1, as written, are merely drawn to non statutory descriptive material since the claimed steps are just storing and initializing data in the VHDL technology library data structure and not imparting any functionality or use to the structure (i.e. not a computer program product/method or executable instructions embodied on a computer-readable medium). MPEP 2106 recites the following supporting rational for this reasoning:

> "Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when **employed as a computer component**. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data. **Both types of "descriptive material" are nonstatutory when claimed as descriptive material per se.** Warmerdam, 33 F.3d at 1360, 31 USPQ2d at 1759. When functional descriptive material is **recorded on some computer-readable medium** it becomes structurally and **functionally interrelated to the medium** and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized."

Further, The Examiner submits that method claim 1, as written, are merely drawn to a mental process for updating variable value in a data structure, since the language of the claims can be interpreted as meaning the method is carried out by a mental process augmented (calculating) using pencil and paper. The steps of storing the

tpd_super_fall_time & tpd_super_rise_time and initializing other variables based on an equation (calculation) can all be done on paper. MPEP 2111 states:

> In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969) (Claim 9 was directed to a process of analyzing data generated by mass spectrographic analysis of a gas. The process comprised selecting the data to be analyzed by subjecting the data to a mathematical manipulation. The examiner made rejections under 35 U.S.C. 101 and 102. In the 35 U.S.C. 102 rejection, the examiner explained that the claim was anticipated by a mental process augmented by pencil and paper markings. The court agreed that the claim was not limited to using a machine to carry out the process since the claim did not explicitly set forth the machine. The court explained that "reading a claim in light of the specification, to thereby interpret limitations explicitly recited in the claim, is a quite different thing from reading limitations of the specification into a claim,' to thereby narrow the scope of the claim by implicitly adding disclosed limitations which have no express basis in the claim." The court found that applicant was advocating the latter, i.e., the impermissible importation of subject matter from the specification into the claim.)

Further, method of claim 1, as written, does not achieve any useful, concrete and tangible application. MPEP 2106 states:

> The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." State Street, 149 F.3d at 1373, 47 USPQ2d at 1601-02.

Second rejection for claim 1 can be corrected by bringing the claims into technological arts by using phrases such as, "A computer implemented method of...".

Regarding Claim 2

Method of claim 2, as written, is rejected based on it dependency on claim 1 and additionally rejected based on the same reason as stated with MPEP 2111 above.

Regarding Claim 3

The method of claim 3, as written, is non-statutory as fails to show all 3 criteria: useful, concrete and tangible. There is no use disclosed in the claim for binding the delay constants. Claim 3 is not concrete as there is no assured result emanating from the method step of "binding" and it is not tangible because there is no implementation involved. Further, claim 3 is rejected for same reasons as claim 1 as

having non-statutory descriptive material and step that can be carried out by a mental process augmented (calculating) by pencil and paper.

Regarding Claim 4 & 5

The method of claim 4, as written, is non-statutory because it represents an abstract mathematical idea defining the data structure and transforming the way delay data is contained in an array. MPEP 2106 states:

> - "[T]ransformation of data, representing discrete dollar amounts, by a machine through a series of mathematical calculations into a final share price, constitutes a practical application of a mathematical algorithm, formula, or calculation, because it produces a useful, concrete and tangible result' -- a final share price momentarily fixed for recording and reporting purposes and even accepted and relied upon by regulatory authorities and in subsequent trades." State Street, 149 F.3d at 1373, 47 USPQ2d at 1601;

Further, claim 4 & 5 are rejected based on their dependency on claim 3.

Regarding Claim 6

The method of claim 6, as written, is non-statutory for the same reasons as disclosed in claim 1,3-5 rejections above.

Regarding Claim 10 & 11

The method of claim 10, as written, is non-statutory because it discloses a computer readable medium to consist of "transitory state mediums"/"network circuits", which by current USPTO practices are not defined to be tangible mediums. Further, Claim 11 is rejected based on its dependency on claim 10.

To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. § 101 (nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. **Claims 1-5 & 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over "IEEE Standard for VITAL ASIC Modeling Specification" – IEEE Std 1076.4-1995 (Std1076 hereafter), in view of "Standard Delay Format Specification Version 2.1" by Open Verilog International (OVI2.1 hereafter).**

Regarding Claim 1

Std1076 teaches storing the rise time and fall time generic declarations for every gate model in VHDL model library (Std1076: Pg.62, Section 9.4.1; Pg.19 Section 5.1/5.2 Lines 24-45). Further, **Std1076** teaches initializing and updating other generic variables in the model (Std1076: Pg.20 Lines 11-13). **Std1076** teaches mapping (correlation) between specific timing generics and the standard delay format constructs (Std1076: Pg. 20 Lines 16-31) which contain the delay data.

Std1076 does not teach specifically the correlation policy associated with the delay.

OVI2.1 teaches correlation policy and format for the delay correlation (OVI2.1: Pg. 3-10 to 3-12).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **OVI2.1** to **Std1076** and modify to include correlation policy with the delay formats and mapping them into the **Std1076** standard. The motivation would have been that **OVI2.1** discloses the Standard Delay Format Standard for the standard delay file generated and **Std1076** uses the standard delay file to back annotate and map the delays from the SDF file constructs (OVI2.1: Pg. 3-10 to 3-12; Std1076: Pg. 5 Lines 23-25).

Regarding Claim 2

Std1076 teaches collecting and back annotating timing generics present in the Standard delay File in SDF format. Further, **Std1076** teaches mapping, which is used to select and extract timing from the SDF file and inserted into the VHDL model (Std1076: Pg.6 Lines 38-47).

Regarding Claims 3, 4 & 5

Std1076 teaches binding correlated delay constants in a 3 dimensional variable data array structure to the VHDL library (Std1076: Pg. 23 Lines 15-22; Pg.59-60 Sec 9.1). Although the array disclosed is not 3 dimensional, the 3 axes of the 3 dimensional data array are obvious. The z-axis donates the blocks for given gate topology. There are multiple versions delays for a single gate topology that can be specified based on the conditions command (Std1076: Pg.27-28, Section 5.2.7.2.1 & 5.2.7.3.2). This is equivalent in functionality and would satisfy z-axis parameter. The x-axis parameter represents the delay name. There are various timing generics representing the delay names taught by the **Std1076** (Std1076: pg.12 Lines 1-5). **Std1076** teaches the y-axis, which represents the actual delay value (Std1076: Pg. 25 Lines 1–14). Further, z-axis data structure represents a generic delay name common to plurality of logic gates (e.g. Tipd for a 2 input gate structure) (Std1076: Pg. 25 Lines 1–14).

Regarding Claims 10 & 11

Claims 10 & 11 disclose the same limitations as claim 1 & 2 and are rejected for the same reasons as claim 1 & 2 respectively.

Regarding Claims 12, 13 & 14

Claims 12,13 & 14 disclose the same limitations as claim 3,4 & 5 and are rejected for the same reasons as claim 3,4 & 5 respectively.

10. Claims 6 & 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over "IEEE Standard for VITAL ASIC Modeling Specification" – IEEE Std 1076.4-1995 (Std1076 hereafter), in view of "IEEE Standard for Integrated Circuit (IC) Delay and Power Calculation System" - IEEE Std 1481-1999 (Std1481 hereafter).

Regarding Claim 6

Std1076 teaches storing the rise time and fall time generic declarations for every gate model in VHDL model library (Std1076: Pg.62, Section 9.4.1; Pg.19 Section 5.1/5.2 Lines 24-45). Further, **Std1076** teaches initializing and updating other generic variables in the model (Std1076: Pg.20 Lines 11-13). **Std1076** teaches mapping between specific timing generics and the standard delay format constructs (Std1076: Pg. 20 Lines 16-31) which contain the delay data.

Further, **Std1076** teaches binding correlated delay constants in a 3 dimensional variable data array structure to the VHDL library (Std1076: Pg. 23 Lines 15-22; Pg.59-60 Sec 9.1). Although the array disclosed is not 3 dimensional, the 3 axes of the 3 dimensional data array are obvious. The z-axis donates the blocks for given gate topology. There are multiple versions delays for a single gate topology that can be specified based on the conditions command (Std1076: Pg.27-28, Section 5.2.7.2.1 & 5.2.7.3.2). This is equivalent in functionality and would satisfy z-axis parameter. The x-axis parameter represents the delay name. There are various timing generics representing the delay names taught by the **Std1076** (Std1076:

pg.12 Lines 1-5). **Std1076** teaches the y-axis, which represents the actual delay value (Std1076: Pg. 25 Lines 1–14).

Std1076 does not teach generic declarations consisting of pointer and resolving the pointer at link-time.

Std1481 teaches delay calculation language (DCL) where generic declaration associated to delay data contains pointer (Std1481: Pg.4 Sec 3.20; Pg.20 Cell_Data; Pg.21 Path_Data; Pg.30 Sec 6.7.1). Further, Std1481 teaches resolving the pointer at link time (Std1481: Pg.4 Sec. 3.17).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Std1481** to **Std1076** and handle delays in the disclosed manner. The motivation would to combine would have been that **Std1481** teaches delay calculation pre- and post-layout phases of chip designs done in Verilog and VHDL (Std1481: Pg iii Background ¶ 4). The previously disclosed OVI standard for the SDF files works with **Std1481** and is compatible with DCL (Std1481: Pg iii Background ¶5).

Regarding Claim 15

Claim 15 discloses the same limitations as claim 6 and is rejected for the same reasons as claim 6.

11. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over "IEEE Standard for VITAL ASIC Modeling Specification" – IEEE Std 1076.4-1995 (Std1076 hereafter), in view of "IEEE Standard for Integrated Circuit (IC) Delay and Power Calculation System" - IEEE Std 1481-1999 (Std1481 hereafter), further in view of "Standard Delay Format Specification Version 2.1" by Open Verilog International (OVI2.1 hereafter)

Regarding Claim 7

Teachings of and motivation to combine **Std1076** & **Std1481** are disclosed in claim 6 rejection above. Further, **Std1481** discloses a linking procedure involving memory and a computer-aided engineering (or EDA) environment (Std1481: Pg.4 Sec. 3.17, Abstract –Top page).

Std1076 & **Std1481** do not teach correlation policy.

OVI2.1 teaches correlation policy and format for the delay correlation (OVI2.1: Pg. 3-10 to 3-12).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **OVI2.1** and apply them to **Std1076** & **Std1481** to handle delays in the disclosed form. The motivation to combine would have been that **Std1481** teaches delay calculation for pre- and post-layout phases of chip designs done in Verilog or VHDL (Std1481: Pg iii Background ¶ 4) and works with **OVI2.1.** Also, the previously disclosed OVI standard for the SDF files works with **Std1481** and is compatible with DCL (Std1481: Pg iii Background ¶5). Further, the motivation to combine **OVI2.1** with **Std1076** would have been that

OVI2.1 discloses the Standard Delay Format Standard for the standard delay file generated. **Std1076** uses the standard delay file to back annotate and map the delays from the SDF file constructs (OVI2.1: Pg. 3-10 to 3-12; Std1076: Pg. 5 Lines 23-25).

Regarding Claims 8 & 9

OVI2.1 teaches VHDL correlation and SDF files (OVI2.1: Pg. 3-10 to 3-12). **Std1481** teaches memory to perform delay calculation operations and **Std1076** teaches analogous 3 dimensional variable data as explained above in the claim 7 rejection. Further, **OVI2.1** teaches that the VHDL correlation data is embedded in the cell as timing properties, which is part of the VHDL package (OVI2.1: Pg.2-7; Pg. ii; Pg.1-4). End of claim rejections.

Conclusion

12. All claims are rejected.

Examiner's Note: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R. Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Friday, July 08, 2005

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